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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,175	12/08/2003	May Xun	CRNG.049(1)	2900

7590 09/15/2005

VOLENTINE FRANCOS, P.L.L.C.
Suite 150
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Reston, VA 20191

EXAMINER	
LOPEZ, CARLOS N	

ART UNIT	PAPER NUMBER
1731	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

NEW CENTRAL FAX NUMBER

Effective July 15, 2005

On July 15, 2005, the Central FAX Number will change to **571-273-8300**. This new Central FAX Number is the result of relocating the Central FAX server to the Office's Alexandria, Virginia campus.

Most facsimile-transmitted patent application related correspondence is required to be sent to the Central FAX Number. To give customers time to adjust to the new Central FAX Number, faxes sent to the old number (703-872-9306) will be routed to the new number until September 15, 2005. After September 15, 2005, the old number will no longer be in service and **571-273-8300** will be the only facsimile number recognized for "centralized delivery".

CENTRALIZED DELIVERY POLICY: For patent related correspondence, hand carry deliveries must be made to the Customer Service Window (now located at the Randolph Building, 401 Dulany Street, Alexandria, VA 22314), and facsimile transmissions must be sent to the Central FAX number, unless an exception applies. For example, if the examiner has rejected claims in a regular U.S. patent application, and the reply to the examiner's Office action is desired to be transmitted by facsimile rather than mailed, the reply must be sent to the Central FAX Number.

Office Action Summary	Application No.	Applicant(s)	
	10/733,175	MAILE ET AL.	
	Examiner	Art Unit	
	Carlos Lopez	1731	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recited of modifying a thermal stress such that the thermal stress is a tensile stress or a substantially zero in a specific temperature range. The claim does not specify the material for which its thermal stress is specified. What material has its thermal stress modified?

In claim 1, is the phrase "a thermal stress", and "tensile stress" referring to any glass or the glass that is being cooled?

eliminates damage due to thermal distortion, hence the cooling treatment modifies thermal stress in the glass sheet to substantially zero.

As for claim 3 as best shown in figure 4, the 30th and 5 hour duration have different slopes.

As for claim 4, the claimed third slope is deemed as the cooling rate when the glass sheet arrives to room temperature for which the glass sheet remains at room temperature proving a slope of zero, no change in the temperature of the glass sheet.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda (JP 10-053426) in view of Kitayama et al (US 5,916,656). Maeda discloses a method of making glass for optical recording mediums (See Machine translation paragraph 1). The method comprises drawing glass (as shown in figure 1) and cooling the glass by passing the glass into a segmented cooling device comprising 12 compartments (see machine translation paragraph 30 and figure 3). Maeda is silent disclosing modifying a thermal stress of the glass sheet such that the thermal stress is a tensile stress or substantially zero. However, Maeda notes that the glass manufactured

by its method provides for glass having a small curvature, which is deemed as being substantially free from warping (See Machine translation paragraph 34). The small curvature noted by Maeda is due thermal stress caused by the varying temperature within the glass, thus in providing a glass having a small curvature, Maeda is in fact modifying, minimizing, the thermal stress of the glass. As further taught by Kitayama, glass used for optical recording mediums, as done by Maeda, is preferred to have no thermal distortion (Col. 23, lines 1ff), no thermal stress.

Thus, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have provided a glass sheet of Maeda having no warping as alluded by Maeda itself and further taught by Kitayama in order to provide a glass for optical recording medium.

As for claim 2-4, 12-13, 16, 19-20, and 22-23 the molten glass sheet, hence at a temperature in its glass transition range, passing through 12 compartments each having a temperature difference of at least 10 degrees celcius (See Machine translation paragraph 30) provides for the claimed cooling segments having different slopes and as noted in machine translation paragraph 31, the temperature of the cooling is done over the glass transition temperature of the glass, 500°C.

As for claims 6-7, 17, and 24 the temperature of each segments is lowered by a difference ranging from 10°C to 40°C, thus the slope of a segment is higher the preceding segment.

As for claim 8-9, 14, 21, and 25 the glass entering a segment having a lower temperature would cause the segment to increase its temperature for which it would

result in a non-linear cooling as evidenced by Newton's cooling equation, see non-patent literature cited in PTO-892.

As for claim 10, the glass being drawn downward towards gravity is under tension.

As for claim 11, a repetition of the processes disclosed by Maeda, would have been done to arrive at the claimed cooling sequence that would provide a glass with no warping.

As for claim 18, the root is deemed as shaping form 2 of Maeda.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references not applied in the above art rejections have been cited to show the state of the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlos Lopez whose telephone number is 571.272.1193. The examiner can normally be reached on Mon.-Fri. 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Griffin can be reached on 571.272.1189. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CL

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
CRNG.049(1)	10/730,175
Applicant(s)	
May Xun et al.	
Filing Date	**Group Art Unit**
12/8/2003	Unknown

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
CL		10-053426	24.02.1998	Japan			X	

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EXAMINER	DATE CONSIDERED
L Z	9/7/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Notice of References Cited	Application/Control No. 10/730,175	Applicant(s)/Patent Under Reexamination MAILE ET AL.	
	Examiner Carlos Lopez	Art Unit 1731	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,916,656	06-1999	Kitayama et al.	428/64.1
	B	US-3,607,183	09-1971	Flori, Jean Francois	65/83
	C	US-3,914,118	10-1975	Brooke et al.	65/95
	D	US-2003/0233846	12-2003	Boaz, Premakaran T.	65/114
	E	US-2002/0038558	04-2002	Nakata et al.	65/29.19
	F	US-3,536,463	10-1970	MICHALIK EDMUND R; et. al.	65/95
	G	US-3,149,949	09-1964	DOCKERTY STUART M; et. al.	65/53
	H	US-6,772,610	08-2004	Albrand et al.	65/162
	I	US-5,837,026	11-1998	Sugawara et al.	65/66
	J	US-4,913,720	04-1990	Gardon et al.	65/114
	K	US-3,301,650	01-1967	WARD CECIL R	65/95
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Malhammer, AKe, Coooling Efficiency Concept, retrived from http://www.coolingzone.com/Guest/News/NL_NOV_2001/Ake/Nov_Ake_2001.html on 9/7/05.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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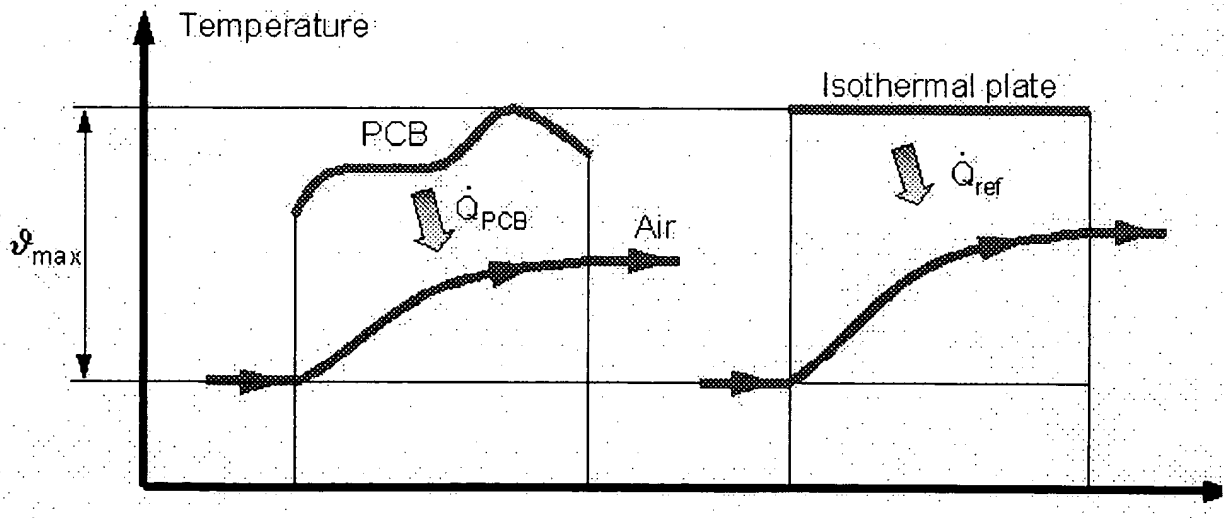
The Cooling Efficiency Concept part 1

Introduction

The cooling efficiency concept has been used for more than 10 years and its effectiveness has been prove in hundreds projects. It is however still only practised by a small minority of thermal designers but in this group it is regarded as key concept. The reasons for this will hopefully become apparent in this and the following expose on the subject.

There are three major employment areas for the concept: as a meter on how well the PCB surface is used for cooling, for thermal estimates and for thermal specifications. Each of these matters represents both important and frequent activities in thermal design. The fact that the cooling efficiency concept can facilitate them considerably should therefore be an important incitement for thermal designers around the world to learn more about the subject.

The first part of this presentation deals with the definition and the importance of temperature criterions. The next part will deal with various forms of applications



$$\eta_c = \frac{\dot{Q}_{PCB}}{\dot{Q}_{ref}}$$

$\dot{Q}_{PCB}$ = heat flow from PCB

$\dot{Q}_{ref}$ = heat flow from reference case

ϑ_{max} = maximum board temperature difference

Figure 1
Definition of the cooling efficiency

Definition

The cooling efficiency is defined as the ratio of the heat that can be dissipated from a PCB and a reference case. The reference case is defined as an ideal smooth isothermal parallel plate case with a temperature level that equals the maximum temperature of the PCB plate, figure 1.

Quite apparent other requirements for the reference case is that the plates must have the same size, thickness, surface-to-surface distance and air flow as the PCB. What might be less apparent, is that it mus not include radiation.

Basic equations

The origins of various heat transfer equations are in most cases quite irrelevant to the application engineer is sufficient to know that they work and when they can be applied. To fully understand the cooling efficiency concept it is however important to go to the bottom of things.

The generally accepted way to characterise convection is to use a heat transfer coefficient. What may have escaped some minds is that the basic formulation for all types of convection, often called Newton's cooling equation, actually mirrors a definition.

Figure 2 shows the fundamental equations involved in the cooling efficiency definition and how it is possible to create an equation that exactly predicts the heat dissipated from a PCB.

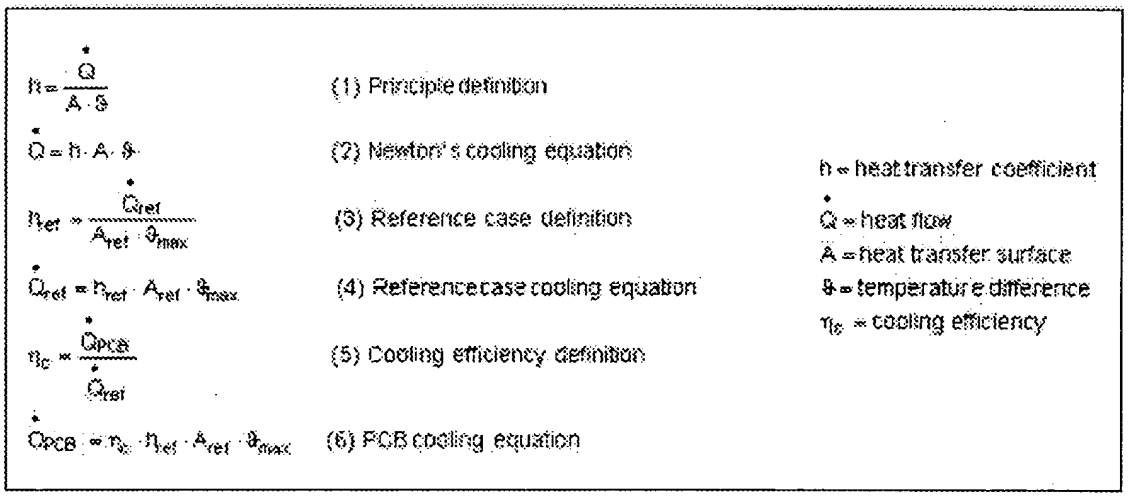


Figure 2
The cooling efficiency definition makes it possible to create an equation that exactly predicts the heat dissipated from a PCB.

Equation 1 is the general definition for the heat transfer coefficient. The parameters involved are not exactly defined. This equation should therefore be regarded more as principle declaration than an expression that actually can be applied. Equation 2 is Newton's cooling equation, which simply mirrors equation 1.

Equation 3 is also a definition of the heat transfer coefficient but in this case with the difference that its parameters are clearly defined. Equation 4 follows from equation 3.

Equation 5 is the definition of the cooling efficiency and it should be kept in mind that it only is valid if the conditions discussed above are fulfilled.

Equation 6 is a combination of equations 4 and 5. It is important to note that this equation is a logical consequence of two definitions. Since a definition by definition always is true, it follows that equation 6 mus be true. It can therefore not be criticised for what it is but it can of course always be criticised for being purposeless or impractical. Part 2 of this expose will therefore essentially be a list of arguments why this nc is the case.

The fact that equation 6 is exact is important. All errors that appear when it is applied must therefore originate from errors within its parameters and not from the equation itself. This is a great strength and one apparent consequence is that it can be used for exact specifications.

The temperature difference used for the equations in figure 2 is the inlet temperature difference. This is somewhat unusual. Most heat transfer literature uses the arithmetic or the logarithmic definitions for the parallel plates flow case. Heat transfer coefficient values based on the inlet temperature difference are therefore somewhat difficult to find. The smoothest work around for this problem is to convert available hea transfer coefficients to the inlet temperature difference definition.

A related issue that often pops up is if calculations that involve the cooling efficiency always must be basec on the inlet temperature difference. The answer to this question is that the cooling efficiency can be regard as a correction factor for the heat dissipated from the reference case. How the reference case is calculated has no importance. It is therefore not necessary to use the inlet temperature difference to calculate the reference case but it facilitates things.

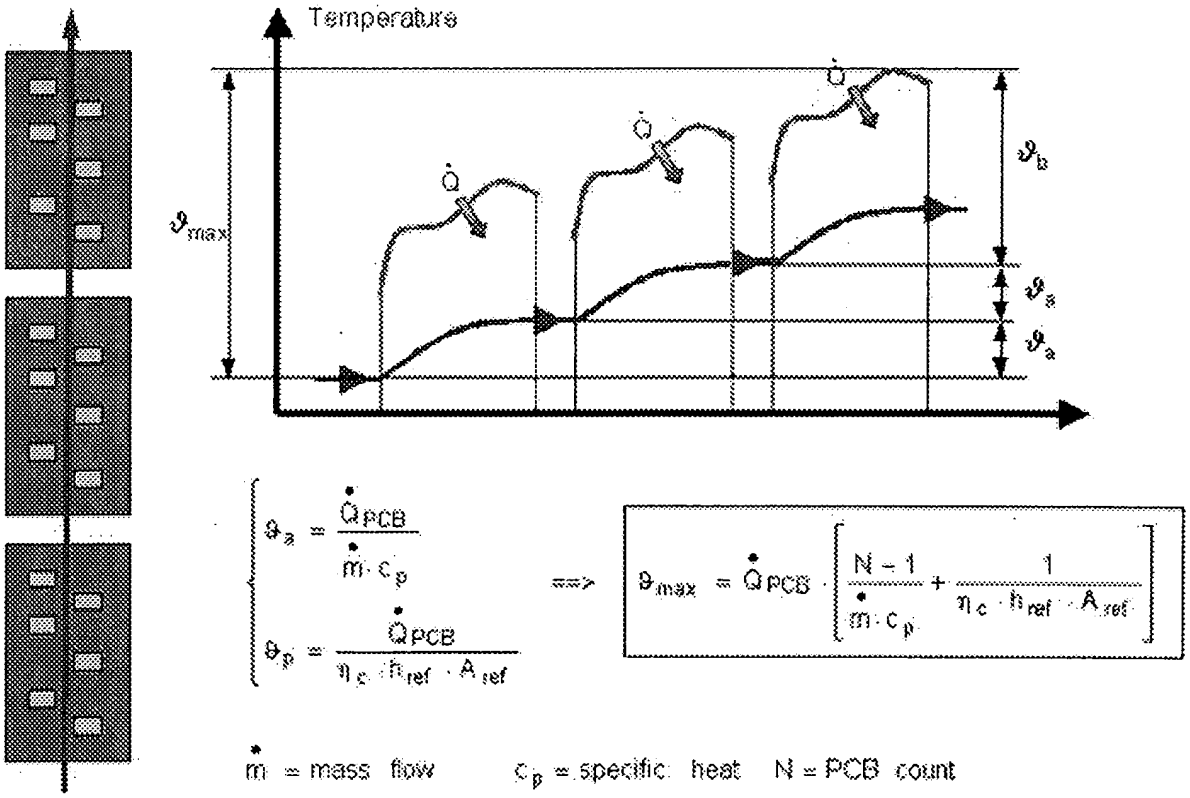


Figure 3
The cooling efficiency applied to a serial cooling case.

Serial cooling

Serial cooling is a term that often is used for cases where the same airflow consecutively cools several PCBs, figure 3. The maximum temperature difference for the top PCB is in these cases composed of two parts. One that accounts for the air temperature increase from the PCBs below and one that accounts for convection from the top PCB.

Figure 3 shows an equation for a simplified case in which it is assumed that all PCBs have the same heat dissipation and pitch. The equation for the general case is slightly more complex.

It should be noted that the maximum board temperature difference in the serial cooling case no longer is proportional to the cooling efficiency. It can therefore be argued that the cooling efficiency concept is more important for single than for serially cooled PCBs.

General results

Copy to clip board Close

Parameter	Dim	Value	Parameter	Dim	Value
Room temp	[°C]	45.0	Fails	[nfails/h]	11042
Air inlet temp	[°C]	50.3	Avg air velo	[m/s]	1.00
Air outlet temp	[°C]	55.7	Radiation cooling	[%]	0.0
PCB average temp	[°C]	70.1	Air efficiency	[%]	22
Max PCB temp	[°C]	94.3	Thermal efficiency	[%]	45
Max pin temp	[°C]	99.1	Cooling efficiency	[%]	61
Max chip temp	[°C]	115.3	Sub rack factor	[–]	1.37
Max comp heat	[W]	1.0	Board factor	[–]	0.44
Heat all over	[W]	4.5			
Total heat	[W]	31.6			

Figure 4

The most practical approach to find a cooling efficiency value is to let a thermal PCB program extract it fro the calculation result.

Cooling efficiency values

The value of the cooling efficiency is given by its definition. There are basically two ways to find it, by measurement or by calculation. The problem with the former method is that the hardware must exist. The problem with the latter method is that there always will be calculation errors. Since the cooling efficiency primarily is used in the design phase, there is not much choice. Almost all cooling efficiency values are therefore calculated. The smoothest approach is to let a thermal PCB program extract them from the calculation result, figure 4. The fact that the reference case is an ideal parallel plates flow case, makes this extraction quite simple.

The quality of the cooling efficiency values obtained in this way is the same as the quality of the calculated temperatures. A benchmark of the program used is therefore also a benchmark of its ability to calculate the cooling efficiency values correctly.

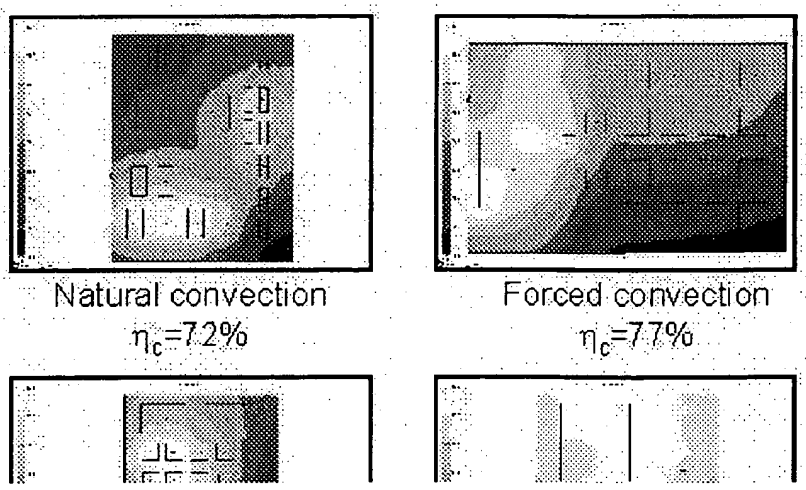


Figure 5
Examples of cooling efficiency values.

Figure 5 shows some examples of calculated values for multi-layer PCBs. It is striking that the values are relatively high, which is a strong argument for the PCB oriented thermal design approach.

Everything that makes a PCB deviate from the isothermal reference case will have an impact on the cooling efficiency, positively or negatively. There are many factors that can have an impact in this respect. The two most obvious ones are the thermal conductivity of the PCB plate and the distribution of the heat sources.

It could be tempting to assume that 100% is the maximum limit for the cooling efficiency. This is however not quite the case. Heat sinks can push the value above the 100% limit. Even a plain PCB can, at least in theory also surpass this limit. The reason for this is that the cooling efficiency is based on the maximum board temperature. The surface temperatures of the components are however frequently higher. The components on a high density PCB can therefore boost the heat dissipation to such an extent that they more than counterbalance the low board temperatures found between the components.

The highest cooling efficiency value that the author has seen for a PCB without heat sinks, is 102%. A student in a training class created it and the lay out was in this case totally free from any other considerations than the thermal ones. The highest corresponding value for an actual design is 90%. It was made by a PCB designer who took a great pleasure in challenging the author's rule of thumb that cooling efficiencies above 80% are almost impossible to achieve without some kind of surface extension.

Heat radiation exchange with the sideboards can also alter the cooling efficiency significantly. This impact is most accentuated in natural convection. In extreme cases it can change the cooling efficiency as much as 30%.

A phenomenon that will change the order of the values disused above, are the air disturbances that are created in the inlets to modern EMC-shielded sub racks? These shields can create massive vortex formations that increase the heat transfer coefficient as much as 60%, even if 30% is more typical. There is not yet sufficient data available to discern more precise numbers. This phenomenon must nevertheless result in a general increase of the cooling efficiency.

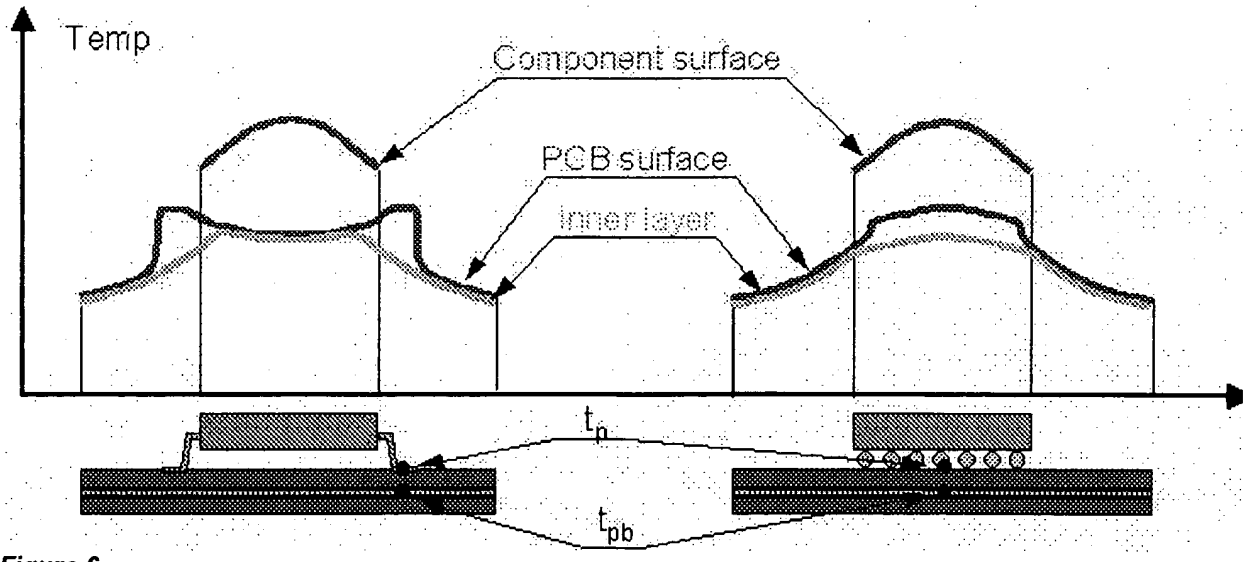


Figure 6
Temperature conditions below components.

Board temperature

The board temperature concept appears with an increasing frequency in the electronics cooling literature. I

is a well-found name for the temperatures on PCBs in general but it is too vague for calculation purposes.

Figure 6 shows two examples of temperature profiles below components. The inner ground and voltage layers, which contrary to the signal layers are almost intact, carry the main part of the heat that is spread o on a PCB. The heat that is pushed down into a PCB must therefore first overcome the thermal resistance caused by the thin layer of basic PCB material that separates the surface pads from the inner layers.

This resistance it not negligible. It is in fact sometimes of the same order as the inner thermal resistances i the component. The temperature on the pads can therefore be significantly higher than the temperature of the inner layer. Some cases are even so critical that the component manufacturer recommends the user to create a certain number of extra thermal connections between the pads and the inner layers, so called thermal vias.

The temperature outside the pads declines very fast towards the inner layer temperature. The properties o PCB material and the critical length of the signal lines emerging from the pads, determine this gradient. Th critical length of a signal line is the length at which its temperature is almost the same as the inner layer temperature. For typical PCBs it is of the order a few millimetres. The surface temperature gradients in the vicinity of a component are therefore normally quite steep.

As indicated in figure 6 it is reasonable to operate with two board temperatures below components. One th is representative for the pads, t_p, and one that is representative for the inner layer temperature below the pads, t_{pb}. It is also good practice to let the way a thermal component model is connected to the PCB reflec this, figure 7.

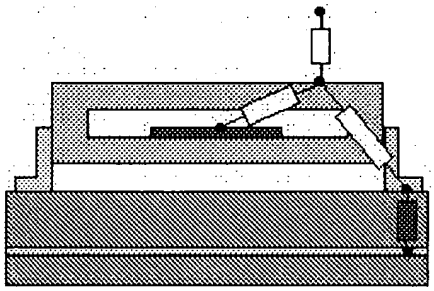


Figure 7
The difference between the PCB surface and the inner layer temperature below a component should be reflected in the way its thermal component model is connected to the PCB.

The board temperature as thermal criterion

The cooling efficiency can be used for several different purposes. One obvious purpose is as a meter for how well the PCB surface is used as a heat sink. This employment is relatively uncomplicated and does nc require any thermal criterion. Other purposes, for example to estimate the maximum heat dissipation that can be allowed on a PCB, can not be made without a board temperature limit.

The cooling efficiency is defined for the temperature difference given by the maximum inner layer temperature, t_{pb}, with the nomenclature used above, and the inlet temperature of the air. There are at least two problems associated with this definition. The first and most important one, is whether it is reasonable t base a thermal design on a board temperature criterion. The second one, is the measurement problem.

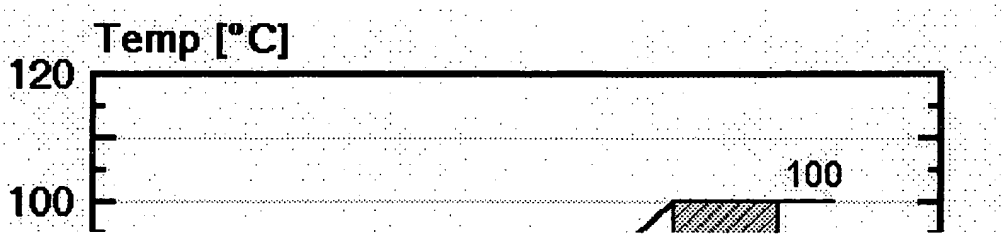


Figure 8
An example on how temperature limits can be specified.

Figure 8 shows an example of a how temperature limits can be specified. Although this particular example many aspects has been overridden by the rapid development of modern hardware, it still reflects the fundamentals. What is somewhat unusual with these limits, is that they not only specify a chip temperature limit but also pad temperature limit.

There are several arguments for why the maximum pad temperature should be limited. They are about iter such as solder point fatigue and PCB discoloration. It is far beyond the author's expertise to evaluate these An argument the author understand however, is that the passive components that often surrounds active components not can be allowed to overheat.

What is of outmost importance is the level of the pad temperature limit. If the pad temperature limit for the safe function case in figure 8 was set to 75 °C instead of 85 °C, the available temperature difference would decrease from 35 °C to 25 °C and the corresponding maximum allowed heat dissipation would decrease w 30%!

An annoying matter is also that the cooling efficiency is defined for the maximum inner layer temperature a not for the maximum pad temperature. This difference is usually not a major concern but it can some times complicate things. A third problem is that the pad temperature not can be measured for modern array type components.

As so many times before, the conclusion of this discussion is that the quality of a calculation procedure ne\ can exceed the quality of the temperature limits.

Conclusions

The definition of the cooling efficiency concept makes it possible to create an exact equation for the heat th can be dissipated from a PCB.

Cooling efficiency values can be extracted from the results calculated by a thermal PCB program. The accuracy of these results equals the accuracy of the program.

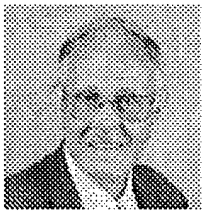
The cooling efficiency values for multi-layer PCBs are often quite high and values above 100% can be achieved if heat sinks are used.

Modern EMC-shielded sub racks create turbulence phenomenon that considerably can enhance the coolin efficiency. There are not yet sufficient experience values available to be more specific about this impact.

Calculations based on the cooling efficiency concept must use a board temperature criterion. It is somewha problematic to determine the quality of that criterion.

It is well motivated to define two types of board temperature below a component. One that is representative for the surface pads and one that is representative for the temperature of the inner layer below the pads.

ABOUT AKE MALHAMMER



Ake obtained his Master of Science degree in 1970 at KTH, (Royal School of Technology), Stockholm. He then continued his studies and financed them with various heat transfer-engineering activities such as deep freezing of hamburgers, nuclear power plant cooling and teaching. His Ph.D. degree was awarded in 1986 with a thesis about frost growth on finned surfaces. Since that year and until December 2000 he was employed at Ericsson as a heat transfer expert. Currently he is establishing himself as an independent consultant.

Having one foot in the university world and the other in the industry, Ake has dedicated himself to applying heat transfer theory to the requirements of the electronic industry. He has developed and considerably contributed to several front-end design methods, he holds several patents and he is regularly lecturing thermal design for electronics.

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In claim 2, 5, 11 and 19, is the phrase "of a glass transition region" referring to any glass or the glass that is being cooled?

In claims 3-8, the term "the cooling" lacks antecedent basis. Additionally, in claims 3-8, and 21-25, the claims refer to "the slope" of the cooling segments, is applicant referring to slope in relation to how the cooling segments are arranged to one another? Or is the term "slope" referring to the temperature vs. distance to the root, wherein the root is the location from which the glass sheet is being drawn?

In claims 8,9,11, and 18, recite "cooling the glass sheet non-linearly", is non-linearly referring to the temperature of the glass?

In claim 18, the phrase "a root" is it referring to the root from which the glass is being drawn or is it to any root?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitayama et al (US 5,916,656). Kitayama discloses method of fabricating a glass sheet (See abstract). The method comprises, as shown in figure 4, the glass sheet is cooled in at least 2 segments wherein in each segment, namely at the 30th and 5 hour duration, the cooling rate, slope varies. As noted in col. 23, line 1ff, the cooling treatment